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Performance Based Comparative Analysis of MOS Structures at 32nm and 20nm Node

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Abstract: MOSFETs have always been the workhorse of semiconductor industry, with passing decades the sizes of MOSFETs have been continuously decreasing. This is guided by decrease in the gate length or channel length. However decrease in channel length of planar MOSFETs has reached its saturation level due to short channel effects and DIBL. In this paper we have tried to present an electrical comparison between 32nm node technology and 20nm node technology of planar MOS structures. The structures have been fabricated using SILVACO TCAD software and study of threshold voltages and corresponding oxide thickness has been made.

Keywords: 35 nmPMOS, 20 nm PMOS, Threshold Voltage, Oxide Thickness, SILVACO TCAD, Athena.

I. INTRODUCTION

The creation of transistor by Walter Brattain, William Shockley and John Bardeen of Bell Labs, New Jersey in the year 1947, proved to be the advent of an entirely new era of technological cosmos. Yet another milestone in this journey was the development of integrated circuits or chips, as they are generally called, with billions of transistors on it and more amazingly each of them functioning perfectly. Consequently, today our elementary cell phones possess more power as compared to supercomputers of the yesteryear. Our cars contain masses of microcontrollers and microprocessors automating every move, be it simple or perplexed. We shop online sitting at our homes and work as well. We recite books on our iPads and Kindles. We play videogames on our personal consoles that are more herculean as compared to flight simulators of twenty years ago.

Smaller MOSFETs are obligatory for several reasons. The most important reason of making transistors smaller is to carton more and more devices in a fixed chip area. This results in a chip with similar functionality in a comparatively small area, or chips with more functionality in the same area. Since fabrication expenses for a semiconductor wafer are relatively fixed, the cost per integrated circuits is primarily related to the number of chips which can be produced per wafer. Hence if the size of IC is small more chips can be manufactured per wafer, hence dropping the price per chip. In fact, since past 30 years the number of transistors per chip has been doubled every 2–3 years on introduction of a new technology node. For example the number of MOSFETs in a microprocessor fabricated in a 45 nm technology is twice as compared to a 65 nm chip. This doubling up of transistor density was first detected by Gordon Moore in 1965 and is frequently referred to as Moore's law.

First, large-scale integration (LSI) fits hundreds of components on top of a single chip and by the 1980's, very large-scale integration (VLSI) became the projecting technology which endorsed hundreds of thousands of components to exist over a single chip. Ultra large-scale integration (ULSI) followed this technology quickly behind yielding millions of components per chip. It also increased their power, efficiency and reliability. The very useful and naturally occurring insulator of silicon, silicon dioxide (SiO_2), acts as a vital part in this size discount due to its terrific ability to offer insulation between components. Many other semiconductor materials do not have such a beneficial instinctive insulating material. As a result, semiconductor circuit production volume has increased tremendously.

The cost of these circuits produced unsurprisingly came down as the technology advanced. A smaller amount of material used is a giant factor in this reduction. The functions performed on several chip and other components can now be performed quicker and with less power dissipation on a much smaller chip. Reduced total manufacturing time also plays a role as the mature fabrication processes are implemented with high-speed and greater volume machines. Price reduction can also be attributed to an increased yield of circuits per silicon wafer resulting from procedures that are cleaner, reproducible and reliable.

Another major advantage that resulted due to the MOSFET was evolution of CMOS (Complementary-Metal-Oxide-Semiconductor) technology. Initially PMOS logic families were exclusively employed because of its high-yield industrial processes. Later, as fabrication condition improved (specifically, airborne particulate and impurity contamination was reduced), NMOS logic circuits became the norm because of their improved performance compared to PMOS technology. More recently, CMOS technology, which employs both PMOS and NMOS transistors, has become very prominent because of its ability to dramatically reduce power dissipation. Essentially, CMOS operates on state switching instead of the common voltage drop model lowering current flow and power loss. This technology can be used to single handedly simulate many different functions. However this was again followed by more its enhanced version as BiCMOS, UltraCMOS and so on.

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The scaling down of conventional planar bulk structure MOSFET has become difficult for gate lengths of 32nm and below. This paper presents comparative analysis of electrical characteristics of Enhancement Mode PMOS fabricated at 32 nm and 20 nm using different materials.

II. STRUCTURE OF PLANAR BULK MOSFET

MOSFET, as represented by its name, is a device working on the concept of Field Effect Transistors (i.e. electrical field generated in the device is responsible for conduction of current through the device). MOS Field Effect Transistors have a layer of SiO_2 acting as insulator and dielectric material on the gate terminal coated with a highly conducting metal like Aluminium, Copper etc. and thus has derived its name as Metal Oxide Semiconductor FET or Insulated Gate FET. The physical structure of planar enhancement type MOSFET is represented in Fig.2.1.

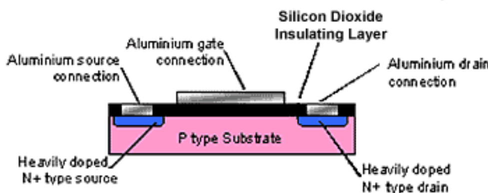

Fig.2.1 Construction of Enhancement MOSFET

A MOS transistor is generally characterized by its gate length (L) & gate width (W). Gate length is the distance; an electron has to travel from highly doped Source to Drain. X-nm refers to the gate length. In the initial period of the MOSFET's development, a gate of 10-micrometer length was a typical design objective. This length would prove to decrease significantly with time and engineers striving to increase speed and component count per unit area. The gate length (the natural measure of the device technology) has been reduced by a factor of 2 about every 5 years. Approximately each lower node technology is "0.7 times the previous technology" i.e. 130 nm, 90 nm, 65 nm, 45 nm etc. The 22 nanometer (22 nm) is the subsequent CMOS process step after the 32 nm stride on the International Technology Roadmap for Semiconductors (ITRS).

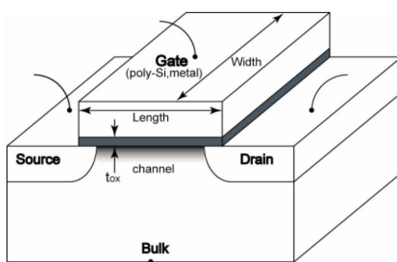

Fig. 2.2 Schematic view of a surface-channel MOSFET device indicating physical gate length, channel width and physical gate dielectric oxide thickness (tox).

Transistor's length, width, and the oxide thickness, each scale with a factor of 0.7 per node. Transistor channel resistance does not change with scaling, whereas gate capacitance is reduced by a factor of 0.7. Therefore, the RC delay of the transistor scales with a factor of 0.7. The chips become faster by 17% per year, reduced power consumption.

Schematically shown in Fig. 2.2, a MOSFET consists of two back-to-back connected *p-n* junctions. The gate voltage applied across metal-oxide semiconductor (MOS) capacitor creates an inversion channel connecting the source and the drain, and controls the carrier density in it. From an operational point of view, the MOSFET has two critical structural parameters, namely gate length and gate dielectric thickness. MOSFET scaling affects both lateral and vertical device dimensions. While the reduction of the lateral dimensions increases the transistor density in a chip, the reduction of the oxide thickness is needed to ensure good electrostatic integrity.In contemporary MOSFETs the drain current *Id* is determined by

$$\frac{I_d}{W} = C_{ox}(V_G - V_{th})v \qquad (1)$$

where$W$ is the channel width, Cox is the gate capacitance per unit area, and v is the source end carrier velocity. The saturation transconductancegmmay be obtained by

$$\frac{g_m}{W} = \frac{\partial I_d}{\partial V_g}/W = C_{ox} \times v = \frac{\epsilon_{ox}}{t_{ox}} \times v \quad (2)$$

where $\varepsilon_{ox}$is the oxide permittivity. The carrier velocity is usually saturated at short-channel MOSFETs, thus g_m/W is an index of gate oxide thickness t_{ox}. Since gate capacitance per unit area is inversely proportional to oxide thickness, both the device current and the saturation transconductance are closely related to oxide thickness.

In addition, the threshold voltage has also been reduced to maintain appropriate gate voltage overdrive according to equation (1). However, the reduction of supply voltage and threshold voltage has lagged the gate length and gate dielectric thickness scaling. The slower reduction of the threshold voltage is due to a combination of factors including increasing channel doping needed to control short-channel effects. The sub linear threshold voltage scaling in turn has retarded the scaling of the supply voltage.

The MOSFET substrate doping, and especially the channel doping concentration, have been continuously increasing since the beginning of scaling. From the original doping density of approximately 2.5×10^{16} cm^{-3} in 1 μm gate length transistors [2], it has already reached more than 2×10^{18} cm^{-3} in contemporary 35 nm gate length MOSFETs.

In MOS devices, the gate dielectric thickness is the single most important device dimension to enable device scaling and has also been the most aggressively scaled one. A thin gate dielectric increases capacitive coupling from the gate to the channel, thereby reducing the source/drain influence on the channel. A larger gate capacitance also leads to a larger inversion charge density, or increased ON-state drive current.

The effects due to scaling down are manifested in various ways:

i) Threshold voltage reduction with decrease in gate length (VT roll-off),

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ii) Drain voltage increases with decrease in threshold voltage (commonly termed as drain induced barrier lowering – DIBL),
iii) Tarnished subthreshold blow.
Collectively, these phenomena are known as ‘short channel effects’ (SCE) and they tend to increase the off-state static leakage power.

III. EFFECTS OF LOWER NODE TECHNOLOGY

Producing MOSFETs with channel lengths much smaller than a micrometer is a challenge, and the difficulties of semiconductor device fabrication are always a limiting factor in advancing integrated circuit technology. In recent years, the small size of the MOSFET, below a few tens of nanometers, has created operational problems

A. *Short Channel Effect*

Short-channel effect is the decrease of threshold voltage in short-channel devices due to two-dimensional (2D) electrostatic charge sharing between the gate and the source drain regions. Short-channel effect plays a key role in -tolerances which determine the minimum acceptable Vt.

B. *Subthreshold leakage*

As voltage that can be applied to the gate must be reduced, the threshold voltage of the MOSFET has to be reduced as well. As threshold voltage is reduced, the transistor cannot be switched from complete turn-off to complete turn-on with the limited voltage swing available thus increase subthreshold leakage.

C. *Increased gate-oxide leakage*

Silicon dioxide has traditionally been used as the gate insulator. Silicon dioxide however has a modest dielectric constant. Increasing the dielectric constant of the gate dielectric allows a thicker layer while maintaining a high capacitance. All else equal, a higher dielectric thickness reduces the quantum tunneling current through the dielectric between the gate and the channel.

D. *Drain induced barrier lowering (DIBL)*

For short channel devices, application of a high drain-to-source bias can lower the threshold voltage and increase the off-currents. This is known as drain induced barrier lowering (DIBL), and is another expression of the short channel effects. Conceptually, drain barrier lowering is caused by the lowering of the potential barrier at the source of a MOSFET due to applied drain bias. There are no known closed form expressions for predicting the threshold shift resulting from DIBL.However, DIBL effects increase with increasing junction depth of the source/drain region.
A measure of DIBL can be defined using the following equation

$$DIBL = \frac{V_{t1} - V_{t2}}{V_{Ds1} - V_{DS2}}$$

where*Vt1* and *Vt2* are threshold voltages at the drain-source voltages *VDS1* and *VDS2* respectively.

E. *Body effect Extraction*

The occupancy of the energy bands in a semiconductor is set by the position of the Fermi level relative to the semiconductor energy-band edges. Application of a source-to substrate reverse bias of the source-body pn-junction introduces a split between the Fermi levels for electrons and holes, moving the Fermi level for the channel further from the band edge, lowering the occupancy of the channel. The effect is to increase the gate voltage necessary to establish the channel, as seen in the figure. This change in channel strength by application of reverse bias is called the *body effect*. The body effect upon the channel can be described using a modification of the threshold voltage, approximated by the following equation:

$$V_{TB} = V_{T0} + \gamma \left(\sqrt{V_{SB} + 2_{\emptyset B}} - \sqrt{2_{\emptyset B}}\right)$$

whereV_{TB} is the threshold voltage with substrate bias present, and V_{T0} is the zero-V_{SB} value of threshold voltage, γ is the body effect parameter, and $2\varphi_B$ is the approximate potential drop between surface.

IV. METHODOLOGY

In this project we have fabricated Insulated Gate FET at 32nm and 20nm gate length technology using Silvaco TCAD. In Silvaco TCAD, ATLAS is a physically-based device simulation program. It predicts the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device into a two or three dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell’s laws, into this grid we can simulate the transport of carriers through such structure. This means that the electrical performance of a device can now be modeled in dc, ac or transient modes of operation.
A device structure can be defined in three different ways for use in ATLAS.
The first way is to read an existing structure from a file. The structure is created either by an earlier ATLAS run or another program such as ATHENA or DEVEDIT. A mesh statement loads in the mesh, geometry, electrode positions, and doping of the structure.
The second way is to use the Automatic Interface feature from Deck-build to transfer the input structure from ATHENA or DEVEDIT.
The third way is the one that has been performed in implementing the simulations in this thesis, where the structures of the devices have been created by using the ATLAS command language.
All structures will be designed in ATLAS in two dimensional modes and corresponding analysis is also done in this simulator.

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V. PLANAR MOSFET DESIGN AT 32NM MODE

The fig. 5.1 below shows the design of MOSFET with gate length 32nm using SILVACO TCAD ATHENA Process Simulator.

This MOS structure is fabricated using boron doped silicon as the substrate material and phosphorous is used for well formation to generate a structure of enhancement type p channel MOSFET having gate length of 32nm.

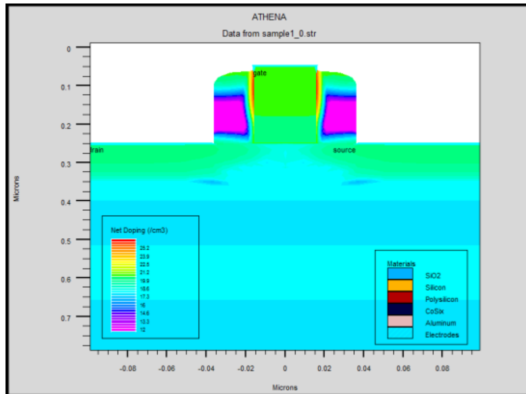

Fig. 5.1 Model of 32nm PMOS

In the above demonstrated figure, MOSFET is having substrate of p type semiconductor with boron as impurity having concentration of $2x10^{15}$. N well of PMOS transistor has been implanted using phosphorous $2.6x10^{13}$.the thickness of gate oxide is 25.3973 angstroms (0.00253973 µm).

The threshold voltage achieved with the device is 0.096969V. Theoutput drain current for various gate voltages is shown below in Fig. 5.2.

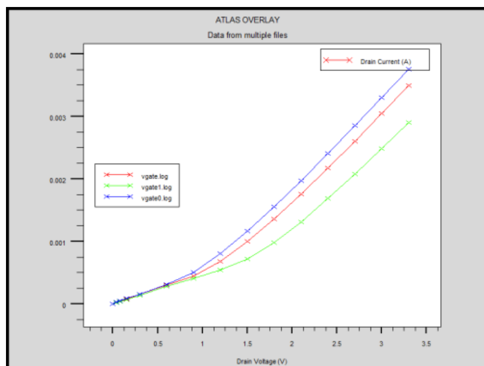

Fig. 5.2 VI Characteristics of 32nm PMOS

VI. PLANAR MOSFET DESIGN AT 20NM MODE

The fig. 6.1 below shows the design of MOSFET with gate length 20nm using SILVACO TCAD ATHENA Process Simulator.

This MOS structure is fabricated using boron doped silicon as the substrate material and phosphorous is used for well formation to generate a structure of enhancement type p channel MOSFET having gate length of 20nm.

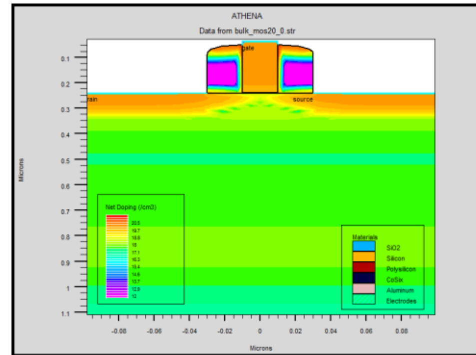

Fig. 6.1 Model of 20nm PMOS

In the above demonstrated figure, MOSFET is having substrate of p type semiconductor with boron as impurity having concentration of $2x10^{15}$. N well of PMOS transistor has been implanted using phosphorous $2.6x10^{13}$. the thickness of gate oxide is 25.4078 angstroms (0.00254078 µm). The threshold voltage achieved with the device is 0.786498V. The output drain current for various gate voltages is shown below in Fig. 6.2.

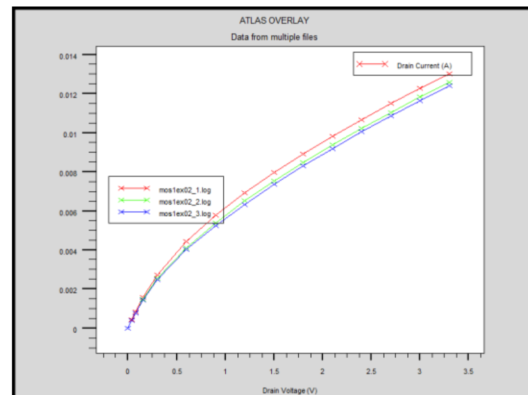

Fig. 6.2 VI Characteristics of 20nm PMOS

VII. CONCLUSION

In this paper we have fabricated Insulated Gate FET or MOSFET at lower node technology of 32nm and 20nm gate length. We have made the comparison of threshold voltage and oxide thickness and its affect on the device characteristics. The graph between bias voltage and drain current has also been plotted.

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